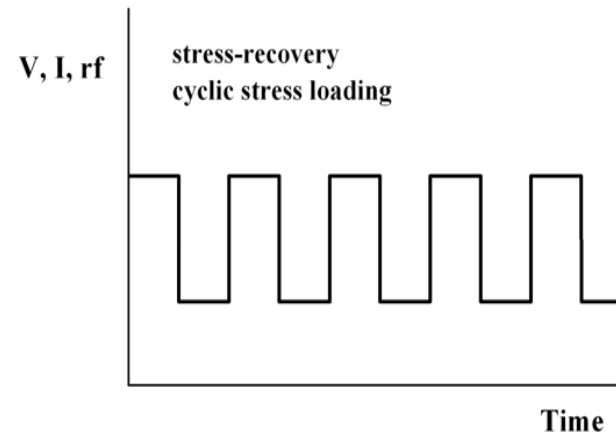
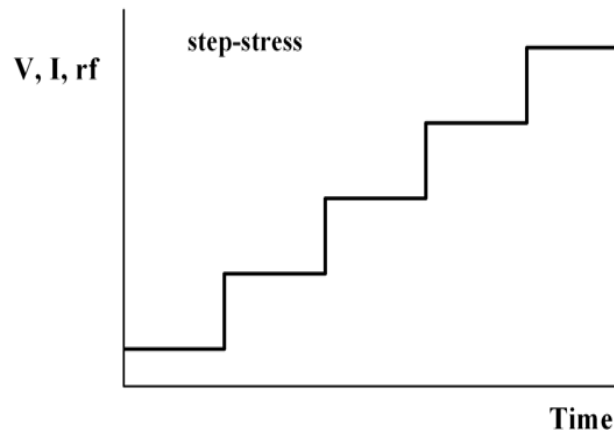


Statistical Support

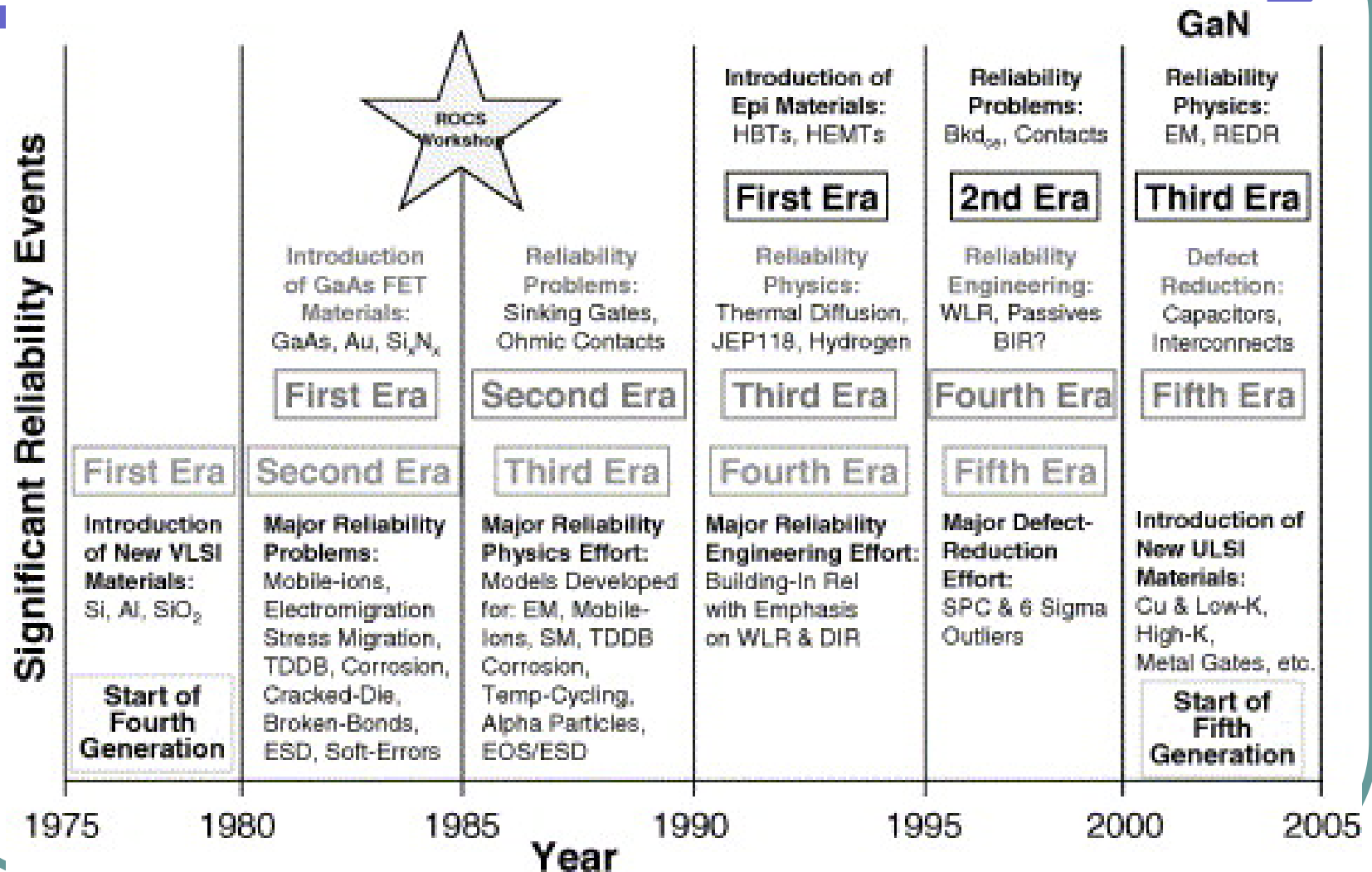
- Basic unit of failure in Si device technology is the FIT(Failure unit),defined as $1 \text{ failure}/10^9$ device hours. For 100 devices on test, a failure rate of 1000 FIT would mean there would be only 1 failure in 1 year.
- Given that a relatively small number of devices will actually show failure, it is critical to both enhance the failure rate through accelerated testing (the five common stresses used are temperature, voltage, current, humidity and temperature cycling) and to treat the resulting reliability data correctly.

Electrical Stress Protocols

- Look for dominant factor causing degradation and is there recovery during OFF-state (trap generation)
- ambient (oxidation, hydrogen effects)
- Field distributions (including inspection of non-uniformity in gate dimensions)
- Visual inspection, dc, rf, base noise spectra (f,V)-check for high leakage, etc.
- Define failure(eg. often 10-20% degradation in HBT current)



Comparisons of silicon and compound semiconductor reliability eras. Silicon eras on the bottom, compound semiconductors across the middle, epitaxial materials are on top (from Roesch 2006 and Stork, 2004)



If CS reliability is to be measured by Si standards, there are 2 focus areas :

1. Formalize the CS knowledge from the initial three reliability eras. Identify, define, and characterize the failure mechanisms for all CS materials. Important to match up the mechanisms with appropriate distributions and acceleration factors, eg. High temperature stress shouldn't be utilized when current density matters! Reliability physics are necessary for all mechanisms, not just when high temperature acceleration is employed.
2. Embrace the tactics of era 4 and 5 quickly and openly. Era 4 means effort on building-in reliability. Need to showcase progress on process control and the search for mavericks, rouge lots, and outliers. Continued development of fast, on-wafer, test structures to speed reliability advancements and new material implementations. Important to apply knowledge of telltale failure signatures and customer returns with the use of in-line screening. Biasing methods of over-voltage, over-current, over-power are expected while quiescent and leakage current monitoring show promise. Hot or cold chuck probing may be needed.

The defect reduction efforts of era 5 offer new territory to apply innovative tactics such as defect amplification, use of new approaches, and/or pioneering accelerations to put CSs ahead of Si.

HEMT Reliability (InP and GaAs)

- Contact problems (esp. sinking gates)
- Surface states (gate lag)
- Hot carrier-induced (impact ionization at gate edge)
- Mechanical stress (H→Ti compressive stress due to piezo effects in semicond, del Alamo 1999)
- Corrosion (fig from Meneghesso and Zanoni, Micro.Rel.42,685 (2002))

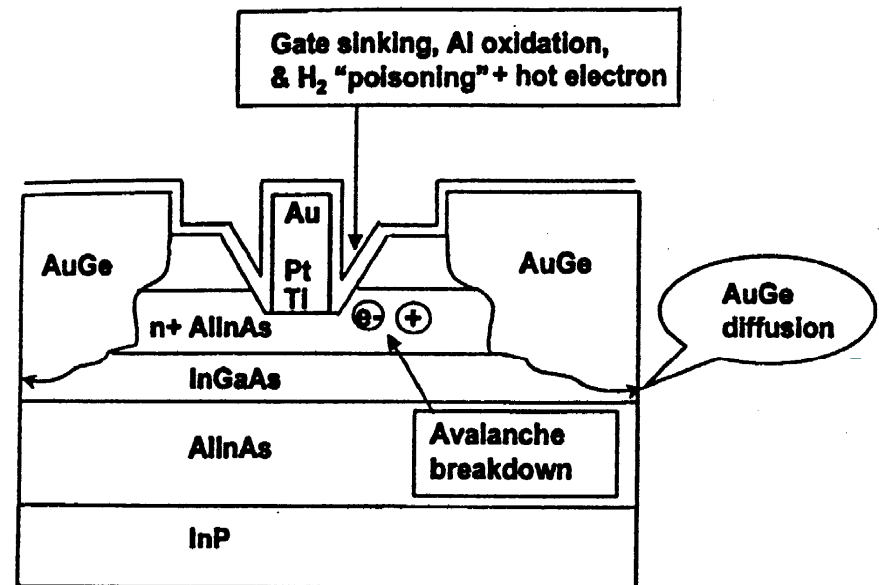
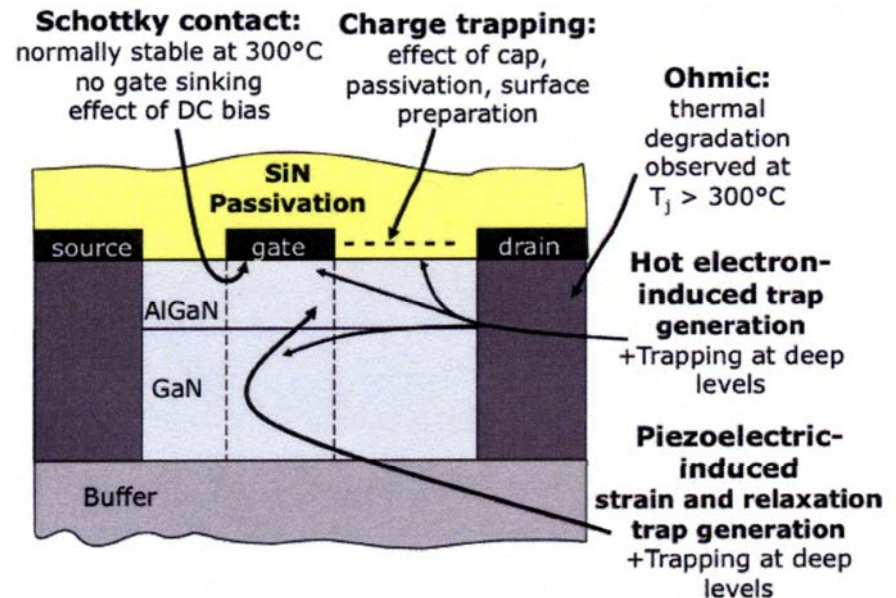


Fig. 1. Schematic cross-section of an InP-based HEMT, identifying the location of possible failure mechanisms.

AlGaN/GaN HEMT Reliability

- Evolution of stress acceleration over the past few years
- 2004 N-G, Chou et al. Micro. Reliab. 44,1033 (2004)
 - step stress 150-240°C 48h, 10 devices
 - degradation starts around 195°C (vendor dependent)
 - I_D , g_m ↓, R_{on} ↑, gate diode unchanged, no metal diffusion
 - at RT, hot electron effects → dc, rf degradation (neg. temp. coeff.)
- 2005 Alcatel, Sozza et al. Micro. Rel. 45,1617 (2005)
 - dc stress (HTRB, HFGC, HTO), 50 devices
 - 3000 h on state (V_{ds} 25V, 6W/mm)/off state (V_{ds} 46V, V_{gs} -6V) hot electron stress
 - ascribed to hot carriers
- 2005, Valizadeh, IEEE Trans DMR 5,555 (2005), noise measurements suggest hot electron degradation
- 2005 HRL Lee et al. Electron Lett. 41(2005), rf stress at 40V, least change for thin AlGaN



AlGaN/GaN HEMT Reliability(cont)

- 2006/2007 Nitronex, Singhal/Piner, Micro.Rel.46,1247(2006)
 - 3 temperature dc data(30,000 device hours, autoclave, ESD,RF life test(4000 h), $E_a=1.7-2.0$ eV, change in barrier height
- 2007 CELAR (France), Burgaud et al.Micro.Rel.47,1653 (2007).
 - rf HTOL, dc HTOL, storage at 200°C GaN-on-Si HEMTs
 - Some gate degradation
- 2007 USC/SET Koudymov et al.,Phys.Stat.Solidi 1,116(2007)
 - rf stress test 50-150°C, E_a 1eV at 150°C to 0.39 eV at 50°C
 - trap generation two orders of magnitude higher at high temperatures.
- 2007-2008 del Alamo, IEEE IEDM,IEEE EDL 29,287(2008)
 - step stress, step recovery and step stress recovery
 - $I_{dmax} \downarrow, R_D \uparrow$, positive shift in V_T ,
 - voltage is main driver, current supplies hot electrons, increases temperature
 - electric field induced defect formation in AlGaN through inverse piezoelectric effect.(AlGaN expands at high fields and total strain may exceed critical value leading to strain relaxation through defect formation)
 - Critical voltage depends on biasing during stressing (higher in off state and high power state than at $V_{ds}=0$),neg depend on stress current-not hot electron induced)
 - Strong forward bias also degrades Schottky junction

AlGaN/GaN HEMT Reliability(cont)

- 2006-2008, Univ. Padova and Modena, Meneghesso, Zanoni et al, IEEE Trans ED 53,2932(2006) and 55,1592 (2008)
- Unpassivated devices on SiC substrates, 10 for each condition, 150 h dc stresses in both on state (open channel $V_{gs}=0V$, $V_{DS}=16V$) and off-state (channel pinched off $V_{gs}=-6V$ and $V_{ds}=32V$)
- Drain current and transconductance decreases, gate lag amplification and reverse gate current decreases
- On state decreased transconductance at high V_{gs} only, off state led to uniform drop over entire V_{gs} range. On state leads to V_t shift due to gate issues
- Differences due to spatial extent of trap formation in gate-drain access region and simultaneous generation of surface and buffer traps, hot electrons in on state stress, strain enhancement and gate-injected electrons contribute in off-state stress.

AlGaN/GaN HEMT Reliability(cont)

- 2007 Northrop Grumman, Coffie et al. IEEE IRPS, pg 568
 - Vds 15-30V, Temp 25-175°C(junction temp 55-205°C, 3 devices each condition, driven at constant 10 GHz input power level(~3 dB compressed)
 - output power degradation $\Delta P_{out}(t)=(1-bt^n)$ where the temp dependence of the fitting parameters b and n were obtained. Both are strongly voltage dependent, the degradation mechanism was not diffusion-limited and a negative activation energy
 - degradation ascribed to hot carrier effects.
- 2007 HRL, Conway et al. IEEE IRPS, pg 472
 - 3 temperature(285,315,345°C) dc step test(48 h 60°C,120 h 120°C) ,burn in (rf stress 175°C) and accelerated rf life test , stressed at 2dB compression with pre rf bias Ids 100 mA/mm, Vds 25V.The rf life test performed at constant channel temperature with 6 devices at each condition.
 - E_a 1.8 eV. Increased current slump after rf stress
- 2007 Univ. Padova, Meneghesso, Zanoni et al.IEDM,IEEE Trans DMR 8,332(2008)
 - dc life tests(3000h),Tj 172°C
 - At moderate drain bias,<30 Vds, hot carrier induced degradation created by trap generation in the gate-drain access region
 - At high drain bias>30-50 Vds, AlGaIn strain relaxation, increase in gate leakage

Statistical Support

- We will use standard Si reliability approaches to determine the instantaneous failure rate and mean time to failure and therefore the distribution functions most relevant to the specific device technology. It is expected that the Weibull distribution is the most relevant, since the failure rate will likely vary as some power of the age of the device. In this case, the failure rate, $\lambda(t)$ is given by

$$\lambda(t) = (\beta/\alpha)t^{\beta-1}$$

where α and β are constants. For $\beta > 1$, the failure rate increases with time, which is likely for compound devices as defect migration/creation, oxidation or contact degradation occur.

- In the early part of our studies, Duane plotting may also be relevant to allow a quick prediction of failure rates when the number of device failures is low. In this approach, the log of the average failure rate (fraction of failed devices at time t divided by the time) is plotted as a function of the log of time. The log-normal distribution function is a more general approach for describing the failure statistics over wide spans of time. It may also be the case that there will be two or more failure populations due to the presence of more than one failure mechanism. This can be resolved on a log-normal distribution that reveals the different time dependence of the various failure mechanisms.

Statistical Support

- Under accelerated aging conditions, different failure mechanisms may be accelerated by different amounts for the same applied stress.
- In Si MOS devices, time dependent failure mechanisms include surface charge accumulation or injection, dielectric breakdown, electro-migration, contact degradation and corrosion due to contamination.
- In compound semiconductors, there are added issues of local regions of non-stoichiometry that affect field distributions and increase recombination, oxidation of AlGaAs or AlGaN, high densities of dislocations and other extended defects in some structures and high surface state densities.

Statistical Support

- We will pay close attention to voltage and current acceleration stress mechanisms. Many studies in Si indicate the reaction rate of the failure mechanism is proportional to a power of the applied voltage as well as temperature, ie

$$R(T,V)=R_o(T)V^{Y(T)}$$

where the coefficient $R_o(T)$ is an Arrhenius function of T and the power dependence varies between 1-4.5. This determines how much acceleration upon increasing the bias voltage used during stressing. If dielectric breakdown is the dominant failure mode, then at a given field, a fraction of the devices will fail in a short time, with no additional failures until an increased field is applied.

- We will consult closely with the reliability statistics experts at Intel and all of the compound semiconductor companies involved in designing stress experiments performed at UF and will work with them to correlate the materials characterization data with the stress conditions they used on devices they provide to UF.

Glossary of terms in reliability

- **THB** (temperature-humidity-bias)-a standard set of conditions defined under Electronics Industry Alliance/JES D22-A101-B. 85°C/85% rel. humidity
- **HAST** (highly accelerated stress test)- a standard set of conditions defined under EIA JES D22-A110B. 110/130°C/85% rel. humidity
- **Burn-in test** -an initial stress at high current or temperature often found to weed-out defective parts and stabilize devices for further test.
- **TLM**-transmission line pattern used for extracting contact resistance- provides larger area for materials analysis. Lateral fields present, vertical fields absent, may be used to identify degrad mechanism in limited cases.
- **SEC**-standard evaluation circuitry
- **MTTF**-median or mean time to failure (time required for 50% population to fail)
- **ESD/EOS**-electrostatic discharge/electrical over-stress. ESD occurs when there is a difference in electrostatic potential between two charged objects; an exchange of electrostatic energy occurs causing their potentials to become balanced. EOS is the term for stress that exceeds the rated V/I and occurs when these exceeds the values guaranteed by the IC.
- **HBM**-human body model; modeling of a situation where energy from an external electrical power or electrostatic energy source becomes charged within the human body to become discharged as electrostatic energy.
- **MM**-machine model; modeling of a situation where electrostatic energy is charged within the machine through a grounding problem or other negative influence.

Glossary of terms in reliability (cont)

- **DIR** –design-in reliability
- **PLR**-package level reliability
- **SPC** -statistical process control using statistical techniques to measure and analyze the variation in processes. Most often used for manufacturing processes, the intent of SPC is to monitor product quality and maintain processes to fixed targets
- **EFR**-early failure rate
- **HTOL**-high temperature operating life
- **HTRB**-high temperature reverse bias
- **HFGC**-high forward gate current
- **Corrosion**- metal degradation due to chemical or electrolytic reactions in presence of moisture, contaminants or bias
- **Electromigration**- movement of metal atoms of a metal line in the direction of the current flow through that line. Metal atoms are removed from the starting end of the metal line and accumulate at the other end, forming voids at the entrance and hillocks at the exit of the line. Electromigration can result in open circuits (due to the voids) or line - to-line short circuits (due to the hillocks). Accelerated by temperature and current density, and is modeled with $t_f = CJ^{-n}e^{(E_a/kT)}$
- **Kink**- abrupt increase in drain current of HEMTs at a certain gate voltage, usually followed by a rapid increase in output conductance. A low frequency phenomenon related to trapping effects.
- **Gate sinking** -reaction of HEMT gate metal with semiconductor at elevated temperatures

Glossary of terms in reliability (cont)

- **COTS**-commercial-off-the-shelf
- **TDDDB**-time dependent dielectric breakdown charge injection mechanism, leading to destruction of dielectric layers over time. During the build-up stage, charges invariably get trapped in various parts of the oxide as current flows in the oxide. The trapped charges increase in number with time, forming high electric fields (electric field = voltage/oxide thickness) and high current regions along the way. This process of electric field build-up continues until the runaway stage is reached. During the runaway stage, the sum of the electric field built up by charge injection and the electric fields applied to the device exceeds the dielectric breakdown threshold in some of the weakest points of the dielectric
- **Gate lag** - a delayed response of the channel current to modulation of the gate potential. Results from traps on semiconductor surface near the gate
- **Hot carrier effects** -phenomenon involving the injection of highly energetic carriers into the gate oxide layer and the substrate, resulting in volume charge build-up that can shift transistor threshold voltages. This mechanism is accelerated by low temperatures. (often observed in HEMTs)-field accelerates electrons in channel. When $E_e > E_g$, impact ionization occurs, creating e-h pairs. Holes flow to the device source, overcome ΔE_v , collected by gate. This leads to a negative gate component which may dominate at high V_{DS} . The shape of the I_G - V_{GS} curves may identify impact ioniz. Manifested by V_T shift, $V_B \uparrow$, g_m and $f_t \downarrow$, power slump
- **BIR** -built in reliability. A phrase used in the Si industry(1900-1995 timeframe) where there was an emphasis on process control, in line screening and wafer level reliability(WLR) testing.